REMARKS

The present application was filed on October 30, 2003 with claims 1-15. Claims 1, 7-9 and 15 are the independent claims.

In an Appeal Decision dated April 17, 2008, the Board of Patent Appeals and Interferences (BPAI) overturned the rejection of claim 15, and upheld the rejection of claims 1-14.

In the outstanding Office Action, in which prosecution was reopened, the Examiner: (i) rejected claims 1-6 and 9-14 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,122,336 to Anderson (hereinafter "Anderson"); (ii) rejected claim 15 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,922,091 to Kizer (hereinafter "Kizer"); and (iii) rejected claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over Anderson in view of U.S. Patent No. 6,295,328 to Kim et al. (hereinafter "Kim").

Although Applicants respectfully disagree with the BPAI's decision for the reasons described in the Appeal Brief filed in conjunction with the above-referenced appeal, Applicants have nonetheless chosen to amend the claims prior to examination without prejudice solely to clarify the claimed subject matter.

By way of example, Applicants have amended independent claim 1 to recite that "the delay element generates a delay signal from the input signal, the delay signal being a delayed form of the input signal, and the phase interpolation circuit generates a first signal by performing a first order interpolation using the input signal and the delay signal, generates a second signal by performing a first order interpolation using the complement of the input signal and the delay signal, and generates a voltage-controlled delay line output signal by performing a second order interpolation using the first signal and the second signal." Similar amendments have been made to the other independent claims. Support for such amendments may be found throughout the present specification, for example, see page 4, line 26, through page 6, line 7.

In the illustrative embodiments described in the above-referenced portion of the present specification, specifically as shown in FIGs. 3A and 3B, the delay element generates a delay signal (Vin') from the input signal (Vin), the delay signal (Vin') being a delayed form of the input signal

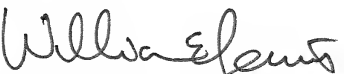
(Vin), and the phase interpolation circuit generates a first signal (V1) by performing a first order interpolation using the input signal (Vin) and the delay signal (Vin'), generates a second signal (V2) by performing a first order interpolation using the complement of the input signal (Vin-bar) and the delay signal (Vin'), and generates a voltage-controlled delay line output signal (Vout) by performing a second order interpolation using the first signal (V1) and the second signal (V2). The tuning range associated with the voltage-controlled delay line shown in FIG. 3A is illustrated in FIG. 3B. As depicted in FIG. 3B, the bottom middle waveform is Vin', which is the delayed waveform of Vin. V1 is generated by phase interpolation (as illustrated in FIG. 3A) using Vin and Vin', and V2 is generated by phase interpolation (as illustrated in FIG. 3A) using Vin' and the complement of Vin. Vout is generated by phase interpolation using V1 and V2. Such tuning range (180 degrees) is advantageously increased over the tuning range shown in FIG. 2B (associated with the voltage-controlled delay line of FIG. 2A). Having the increased tuning range (absolute tuning range of 180 degree) is advantageous to achieve extra tuning margin for target delay requirements.

Applicants assert that neither Anderson, nor Kizer, nor Kim, alone or in combination teach or suggest that the delay element generates a delay signal from the input signal, the delay signal being a delayed form of the input signal, and the phase interpolation circuit generates a first signal by performing a first order interpolation using the input signal and the delay signal, generates a second signal by performing a first order interpolation using the complement of the input signal and the delay signal, and generates a voltage-controlled delay line output signal by performing a second order interpolation using the first signal and the second signal.

Note that Applicants are also filing a revised set of formal drawings, marked "Replacement Sheets," which includes a "Prior Art" legend requested by the previous Examiner in an Office Action dated November 8, 2004.

For at least the above reasons, Applicants assert that claims 1-15 are patentable, and respectfully request withdrawal of the various rejections.

Respectfully submitted,



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